3-V_{RMS} Audio Line Driver with Integrated Charge Pump

Features

- **3-V_{RMS} Output into 2.5kΩ Load with 5V Supply**
- **2-V_{RMS} Output into 2.5kΩ Load with 3.3V Supply**
- **Integrated Charge Pump Generates Negative Supply Rail**
- **SNR Enhanced**
- **PVDD Power Off Delay Function**
- **Low THD+N: 0.001%**
- **Drives 600Ω Load**
- **Stable with 220pF Capacitive Load**
- **Pop-Free Under-Voltage Protection (TPF632A/605A)**
- **Pop-Free Enable Control**
- **–40°C to 85°C Operation Range**
- **Robust 8kV (Output-Pin) HBM ESD Rating On All Pins**
- **Robust 2kV CDM ESD Rating**
- **Green, Popular Type Package**

Applications

- Set-Top Box
- Blue-ray and HD DVD Players
- PDP TV and LCD TV

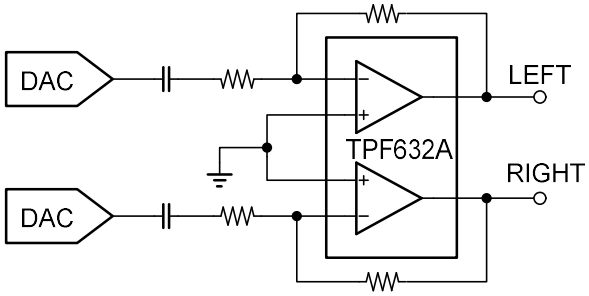


Figure 1. Typical Application Circuit of TPF632A

Description

The 3PEAK TPF632A/605A/607A are 3-V_{RMS} pop-free stereo line drivers with the integrated charge pump generating the negative supply rail which allows the removal of the output DC-blocking capacitors. The devices are capable of driving 3-V_{RMS} into a 2.5-kΩ load with single 5V supply voltage. The TPF632A has differential inputs, the TPF605A/607A support single-ended inputs, and all can use external resistors for flexible gain setting.

The 3PEAK TPF632A/605A/607A has built-in enable/shutdown control for pop-free on/off control. The TPF632A/605A has an external under-voltage detector that mutes the output when monitored voltage drop below set value. Using the TPF632A/605A/607A in audio products can reduce component count considerably compared to traditional methods of generating a 3-V_{RMS} output.

The device needs only a single 5V supply to generate 8.5-V_{PP} output while traditional op-amp requires a split-rail power supply to achieve same. The device is ideal for single-supply electronics where size and cost are critical design parameters.

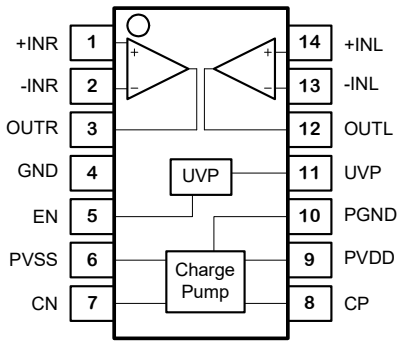
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Audio Line Drivers

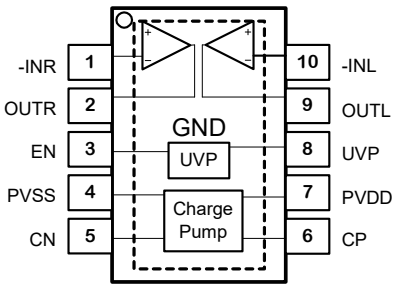
Part Number	Package	Remarks
TPF632A	TSSOP-14	5V/3.3V,Differential inputs
TPF605A	MSOP-10-EP	5V/3.3V, Single-ended inputs
TPF607A	MSOP-10	Single-ended inputs, no UVP control

Pin Configuration (Top View)

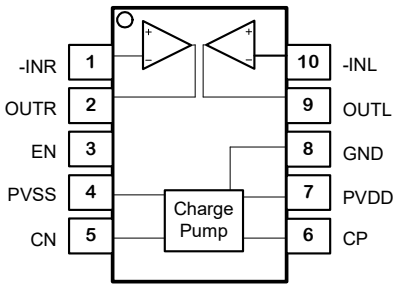
TPF632A
14-Pin TSSOP



TPF605A
10-Pin MSOP-EP



TPF607A
10-Pin MSOP



Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TPF632A	TPF632A-TR	14-Pin TSSOP	Tape and Reel, 3000	TPF632A
TPF605A	TPF605A-VR	10-Pin MSOP-EP	Tape and Reel, 3000	TPF605A
TPF607A	TPF607A-VR	10-Pin MSOP	Tape and Reel, 3000	TPF607A

Absolute Maximum Ratings Note 1

Supply Voltage: $V^+ – V^–$.....6.0V
Input Voltage..... $V^–$ – 0.3 to V^+ + 0.3
Input Current: +IN, –IN, SHDN Note 2..... ±10mA
EN Pin Voltage……$V^–$ to V^+
Output Current: OUT..... ±20mA

Output Short-Circuit Duration Note 3…..... Indefinite
Operating Temperature Range.....–40°C to 125°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Pin	Symbol	Parameter	Condition	Minimum Level	Unit
All	HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	8	kV
All	CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
14-Pin TSSOP	130	49	°C/W
10-Pin MSOP	120	45	°C/W
10-Pin MSOP-EP	70	10	°C/W

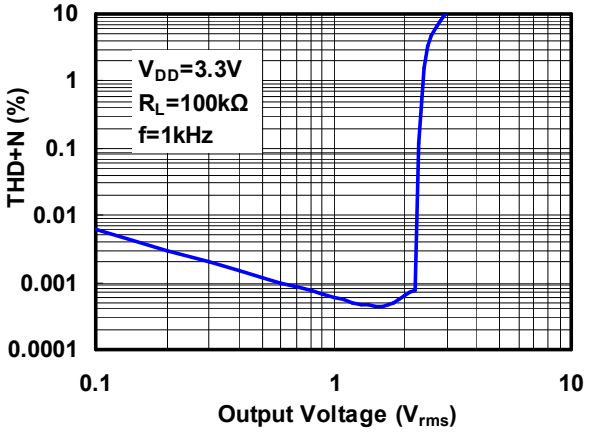
5V Electrical Characteristics

Specifications are at T_A = 27°C. V_{DD} = 5V, R_L = 2.5kΩ, C_{PUMP}=C_{PVSS}=1μF, C_{IN} =10μF, R_{IN} = 10kΩ, R_{FB} = 20kΩ, unless otherwise noted.

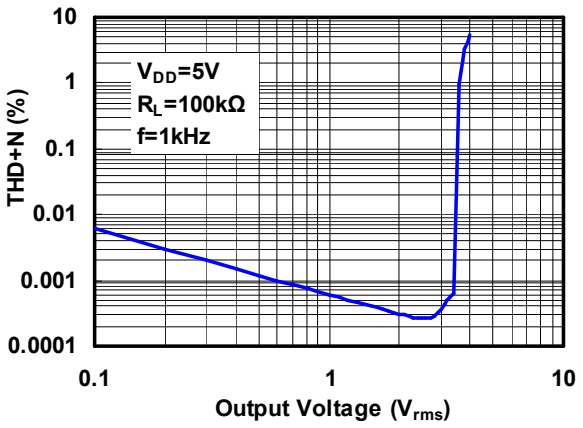
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage Range		2.7		5.5	V
V_{OS}	Output Offset Voltage	Input grounded, unity gain.	-4		4	mV
I_Q	Quiescent Current	No load		4.6		mA
$I_{Q(off)}$	Supply Current in Shutdown				0.2	mA
V_O	Output Voltage	V_{DD}=3.3V, f=1kHz, THD=1%	2.05			V_{RMS}
		V_{DD}=5V, f=1kHz, THD=1%	3.05			V_{RMS}
THD+N	Total Harmonic Distortion Plus Noise	V_O=3V_{RMS}, f=1kHz		0.001		%
V_{ENH}	High-level Threshold Voltage(EN)	V_{DD}=3.3V, EN Low to High Transition	1			V
		V_{DD}=5V, EN Low to High Transition	1			V
V_{ENL}	Low-level Threshold voltage(EN)	V_{DD}=3.3V, EN High to Low Transition			0.5	V
		V_{DD}=5V, EN Low to High Transition			0.6	V
$\|I_{ENH}\|$	High-level input current(EN)	V_{DD} = 5 V, V_I = V_{DD}			0.1	μA
$\|I_{ENL}\|$	Low-level input current(EN)	V_{DD} = 5 V, V_I = 0 V			1	μA
X_{TALK}	Crosstalk	V_O=3V_{RMS}, f=1kHz		-110		dB
I_{SC}	Short Circuit Current	V_{DD}=5V		20		mA
R_{IN}	Input Resistor Range		1	10	47	kΩ
SR	Slew Rate			5		V/μs
C_L	Maximum Capacitive Load				220	pF
C_F	Flying Capacitor		0.1	0.33	2.2	μF
V_N	Noise Output Voltage	BW=20Hz to 20kHz		4.3		μV_{RMS}
SNR	Signal to Noise Ratio	V_O=3V_{RMS}, f=1kHz, BW=20kHz		117		dB
GBW	Unity Gain Bandwidth	No load		10		MHz
A_{VOL}	Open-Loop Voltage Gain	No load		130		dB
V_{UVP}	External Under-voltage Detection	V_{DD}=3.3V	1.18	1.23	1.28	V
		V_{DD}=5V	1.23	1.27	1.30	V
I_{HYS}	External Under-voltage Detection Hysteresis Current			4.7		μA
f_{CP}	Charge Pump Frequency			330		kHz

Typical Performance Characteristics

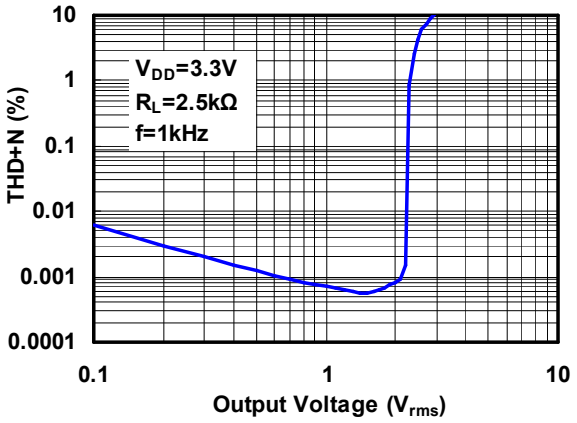
Total Harmonic Distortion + Noise vs. Output Voltage



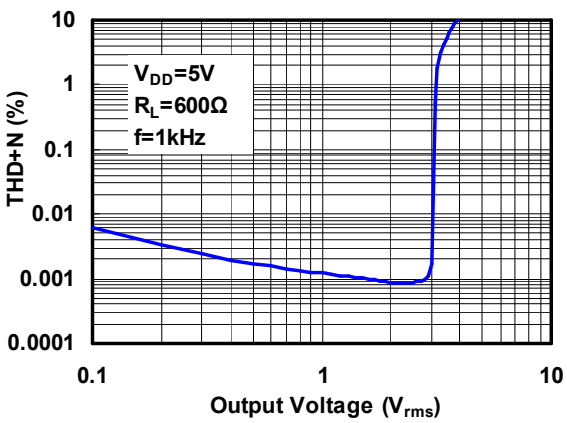
Total Harmonic Distortion + Noise vs. Output Voltage



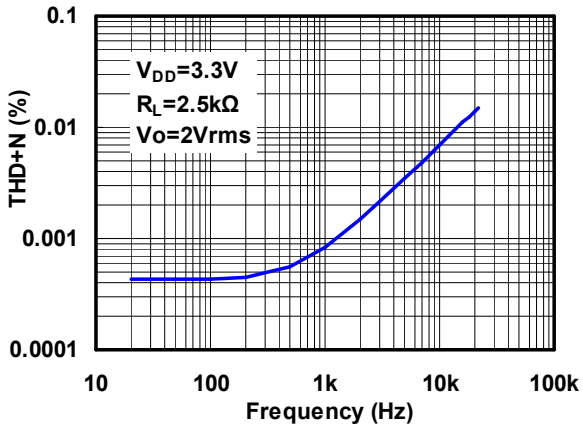
Total Harmonic Distortion + Noise vs. Output Voltage



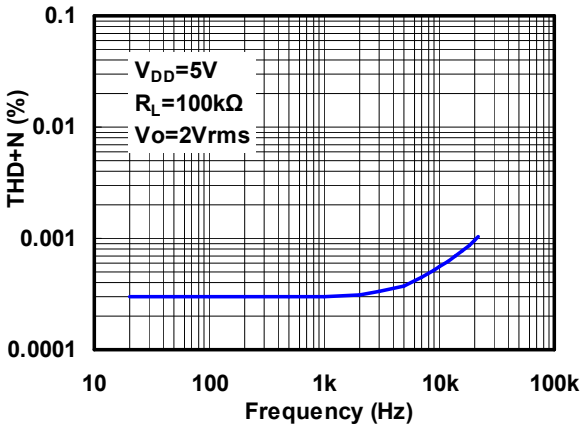
Total Harmonic Distortion + Noise vs. Output Voltage



Total Harmonic Distortion + Noise vs. Frequency



Total Harmonic Distortion + Noise vs. Frequency



Pin Functions

PIN		I/O	Description
Name	Number		
+INR	1	I	Positive input of the right channel OPAMP
-INR	2/1	I	Negative input of the right channel OPAMP
OUTR	3/2	O	Output of the right channel OPAMP
GND	4/EP/8	P	Ground
EN	5/3	I	Enable
PVSS	6/4	P	Negative supply generated with integrated charge pump
CN	7/5	I/O	Negative terminal of the flying capacitor of the charge
CP	8/6	I/O	Positive terminal of the flying capacitor of the charge
PVDD	9/7	P	Positive supply
PGND	10	P	Ground for charge pump
UVP	11/8	I	Under-voltage protection input
OUTL	12/9	O	Output of the left channel OPAMP
-INL	13/10	I	Negative input of the left channel OPAMP
+INR	14	I	Positive input of the left channel OPAMP

Applications Information

Typical Application Circuit

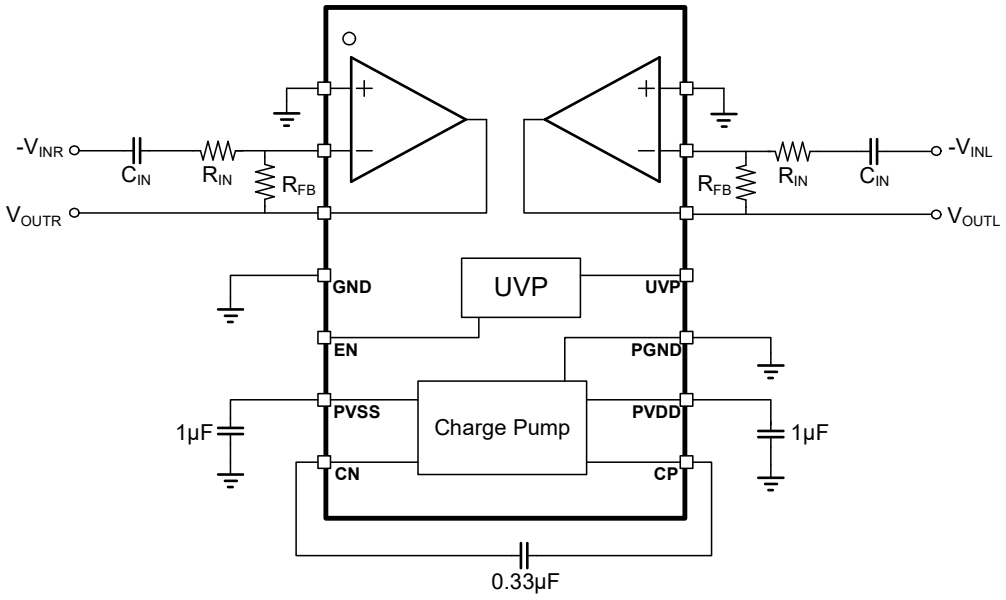


Figure 2 Typical **Application Circuit of TPF632A**

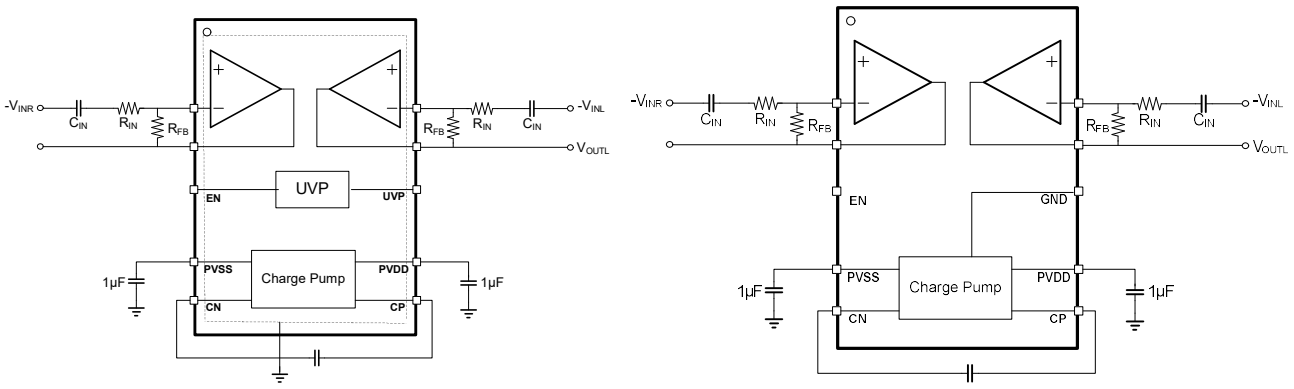


Figure 3 Typical Application Circuit of TPF605A（Left）and TPF607A（Right）

Typical application circuits are shown as above. TPF632A/605A/607A operates from a single supply voltage PVDD. It integrated charge pump generates a negative supply –PVDD at the PVSS pin. The Line driving amplifiers work with dual supplies: PVDD and –PVDD. Therefore, the DC level of the audio output can be designed to be 0V. A DC-blocking capacitor typically seen in a single-supplied driver is not necessary.

The supply range of the TPF632A/605A/607A is 2.7V to 5.5V. For a $3V_{RMS}$ output, the recommended supply voltage is 5V. For a $2V_{RMS}$ output, the recommended supply voltage is 3.3V.

R_{IN} of 2.5kΩ and R_{FB} of 5kΩ set the inverting gain of 2. Because of the exceptional noise performance of TPF632A/605A/607A, the dominant noise source is actually from R_{IN}. To get better noise performance, lower input resistance and feedback resistance may be used.

Integrated Charge Pump

The integrated charge pump in TPF632A/605A/607A generates negative power supply from a single supply PVDD. A flying capacitor for the charge pump shall be applied between CP and CN. At the same time a decoupling capacitor shall be applied between PVSS and ground. Typical value for the flying capacitor is 0.33uF. Typical value of the decoupling capacitor shall be same as or larger than that of the flying capacitor. Low-ESR capacitors are recommended for the flying capacitor and the decoupling capacitor.

Audio Signal Amplification Gain Setting

The main application of the TPF632A/605A/607A is to amplify/buffer audio signals and drive audio lines with very low distortion. Typical application circuits with inverting gain are shown in Figure. 4.

Non-inverting amplification of audio signals is also possible with same low distortion.

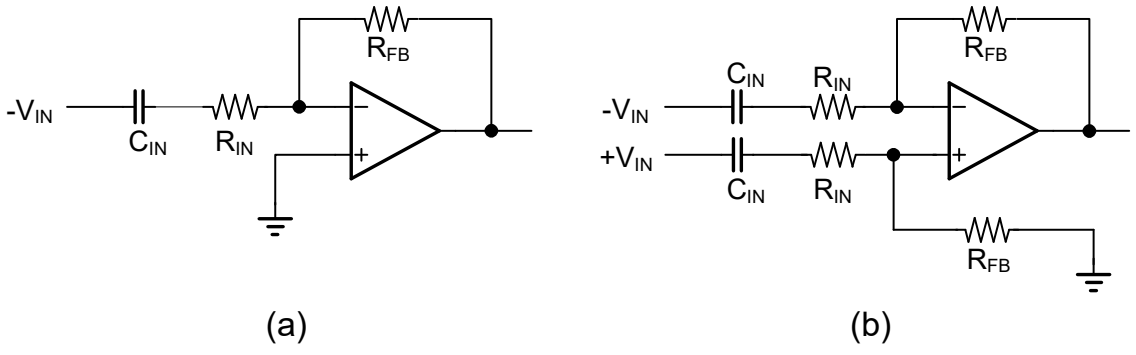


Figure 4 Typical **Application Circuit of TPF632A**

AC-Coupling Input Capacitors

Because of the integrated charge pump that generates negative rail, TP632A/605A/607A may be used to amplify audio signal so the output DC voltage is 0V. This usually requires the DC voltage of the input signal to be 0V. If the input signal has a DC level other than 0V, an AC-coupling capacitor is necessary to block the DC voltage.

The AC-coupling capacitor essentially forms a high-pass filter at the input. The cut-off frequency of the filter has to be low enough not to distort the input audio signal. For an inverting amplifier shown in Figure 4 the cut-off frequency may be calculated as following:

$$f_c = \frac{1}{2\pi R_{IN} C_{IN}} \quad (1)$$

If the required maximum cut-off frequency is known, the minimum AC-coupling capacitance can be determined:

$$C_{IN} \geq \frac{1}{2\pi R_{IN} f_c} \quad (2)$$

Adding Low-Pass Filtering to the Gain

If low-pass filtering is necessary in addition to the audio signal amplification, a second-order filter can be implemented as shown in Figure 5. Choice of C3, R1, R2, and R3 is based on the gain setting requirement and AC-coupling cut-off frequency as discussed above. C1, C2 and C4 may be calculated depending on the bandwidth. Example choices of R and C are listed in Table 1. If first-order filtering satisfies performance requirements, simply remove the C2 and C4 to lower the component counts.

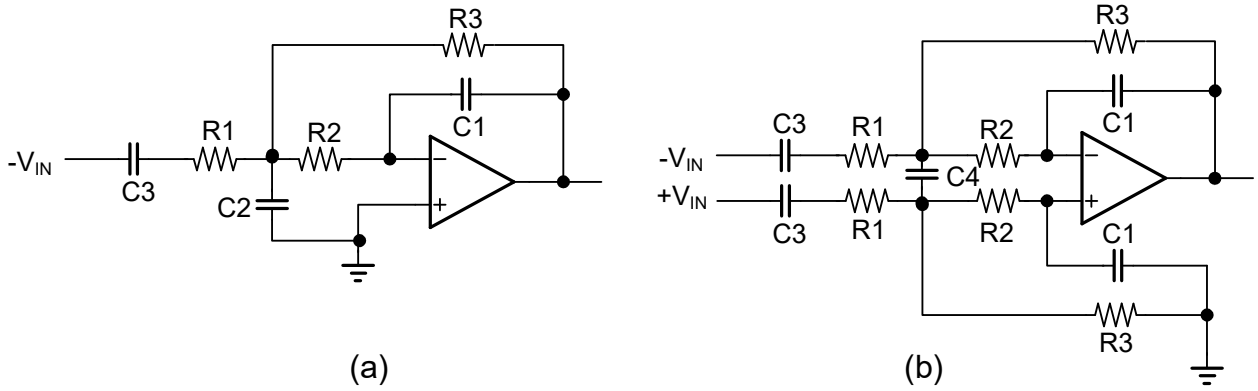


Figure 5 Second**-order filter with gain: (a) Single-ended input; (b) Differential input**

Table 1 Example RC setting at different gains

Gain	R1	R2	R3	C1	C2	C3	C4
G=2	576Ω	549Ω	1150Ω	1nF	6.2nF	100uF	3.1nF
G=2.5	576Ω	412Ω	1430Ω	1nF	6.8nF	100uF	3.4nF
G=3.75	383Ω	301Ω	1430Ω	1nF	9.1nF	100uF	4.5nF

Pop-Free Power Up and Power Down

During power up or power down, the input device that provide audio source may experience significant DC level shift. Charging of the input capacitor due to DC shift will cause pop noise. It is recommended that TPF632A/605A/607A is disabled (EN low) during power up and power down and kept disabled until charging of the input capacitor is complete. The sequence of EN control is illustrated below.

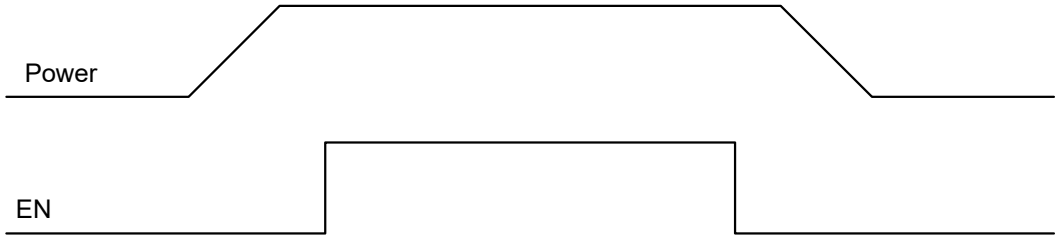


Figure 6 The Sequence of EN Control

Under-voltage Protection

When unexpected power off happens, the host may not have enough time to disable TPF632A/605A/607A before pop noise is generated. The integrated under-voltage protection circuits can be used to mute and disable TPF632A/605A/607A when the monitored supply voltage drops below certain voltage.

The recommended connection is shown below. V_{SUPPLY} is the monitored supply voltage. The threshold voltage at the UVP pin is 1.23V. R3 sets the hysteresis voltage and is usually much larger than R1 and R2. The turn on threshold and hysteresis can be calculated:

$$V_{TH} = 1.23V \times (R1+R2)/R2 \quad (3)$$

$$Hysteresis = 4.7uA \times R3 \times (R1+R2)/R2 \quad (4)$$

$$\text{when } R3>>R1, R2 \quad (5)$$

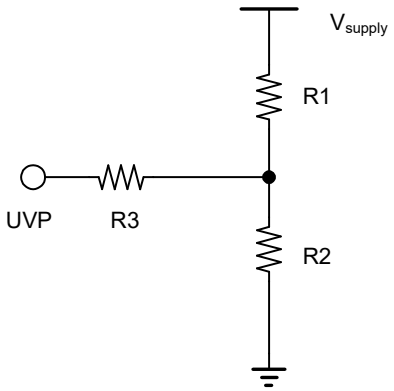


Figure 7 Under-voltage Protection Circuits

ESD

TPF632A/605A/607A has reverse-biased ESD protection diodes on all inputs and outputs. Input and out pins can not be biased more than 300mV beyond either supply rail.

Driving Large Capacitive Load

TPF632A/605A/607A is designed to drive large capacitive loads up to 220pF directly. When driving larger capacitive loads with the TPF632A/605A/607A, a small series resistor at the output (R_{ISO} in Figure 8) improves the feedback loop's phase margin and stability by making the output load resistive at higher frequencies. Usually R_{ISO} of 50Ω is sufficient.

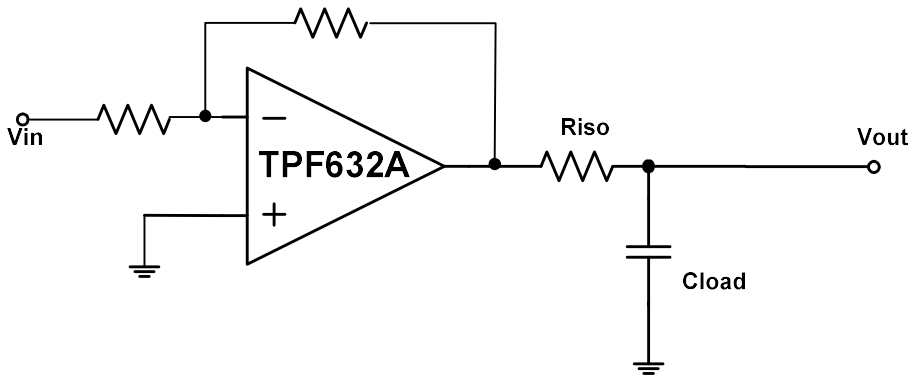


Figure 8 Driving Circuits

Power Supply Layout and Bypass

The power supply pin of TPF632A/605A/607A should have a local bypass capacitor (i.e., 0.01μF to 0.1μF) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1μF or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA's inputs and outputs. To decrease stray capacitance, minimize PC board lengths and resistor leads, and place external components as close to the op amps' pins as possible.

Proper Board Layout

To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

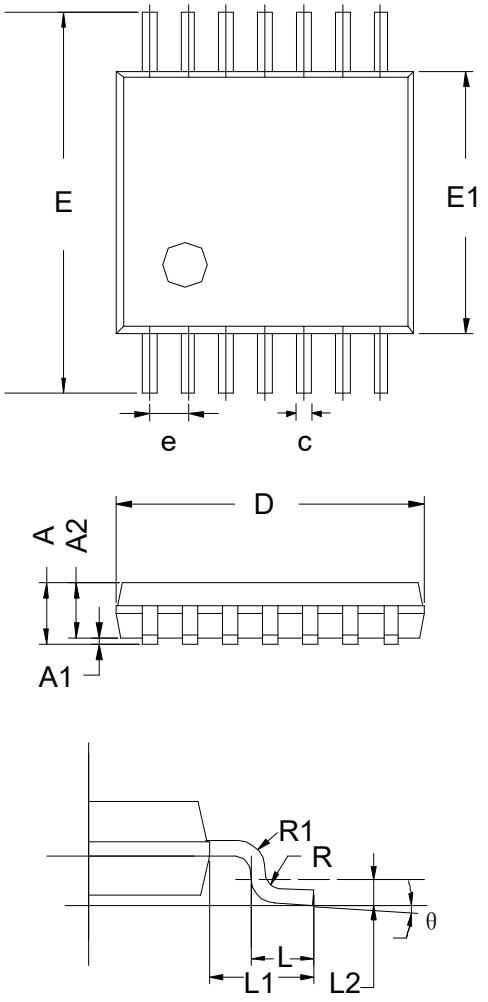
Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

Package Outline Dimensions

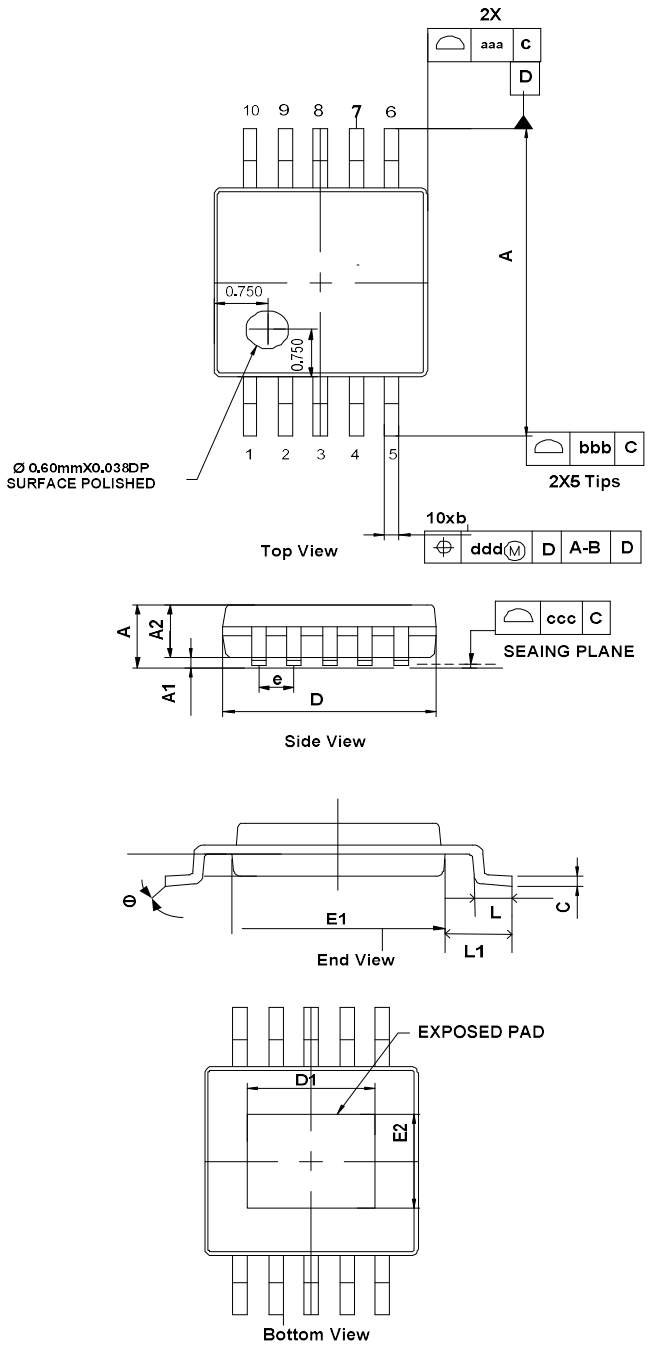
TSSOP-14



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
b	0.20	-	0.28
c	0.10	-	0.19
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
θ	0°	-	8°

Package Outline Dimensions

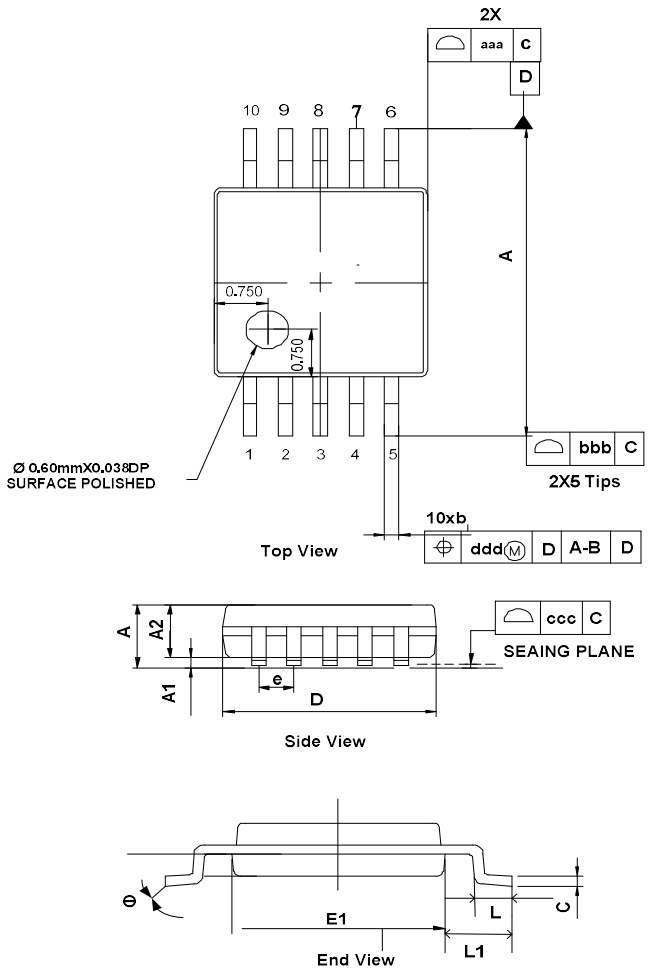
MSOP-10-EP (EXPOSED PAD)



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	-	-	1.10
A1	0.05	-	0.15
A2	0.75	0.85	0.95
b	0.19	-	0.28
c	0.08	0.15	0.23
D	2.90	3.00	3.10
D1	1.80REF		
E1	2.90	3.30	3.10
E2	1.55REF		
e	0.50BSC		
L	0.40	-	0.70
L1	0.95BSC		
θ	0°	-	8°
aaa	0.2		
bbb	0.25		
ccc	0.10		
ddd	0.08		

Package Outline Dimensions

MSOP-10 (NO EXPOSED PAD)



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	-	-	1.10
A1	0.05	-	0.15
A2	0.75	0.85	0.95
b	0.19	-	0.28
c	0.08	0.15	0.23
D	2.90	3.00	3.10
D1	1.80REF		
E1	2.90	3.30	3.10
E2	1.55REF		
e	0.50BSC		
L	0.40	-	0.70
L1	0.95BSC		
θ	0°	-	8°
aaa	0.2		
bbb	0.25		
ccc	0.10		
ddd	0.08		